

Ensemble RXTX 04_Dividers

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Dividers Introduction

Theory of Operation

The Dividers stage takes in the local oscillator's signal and divides it by 4, producing two output signals. Each output signal is at a frequency that is $\frac{1}{4}$ the stage's input signal and is a square wave with 50% duty cycle. The 50% duty cycle is with respect to the regular 5V rail.

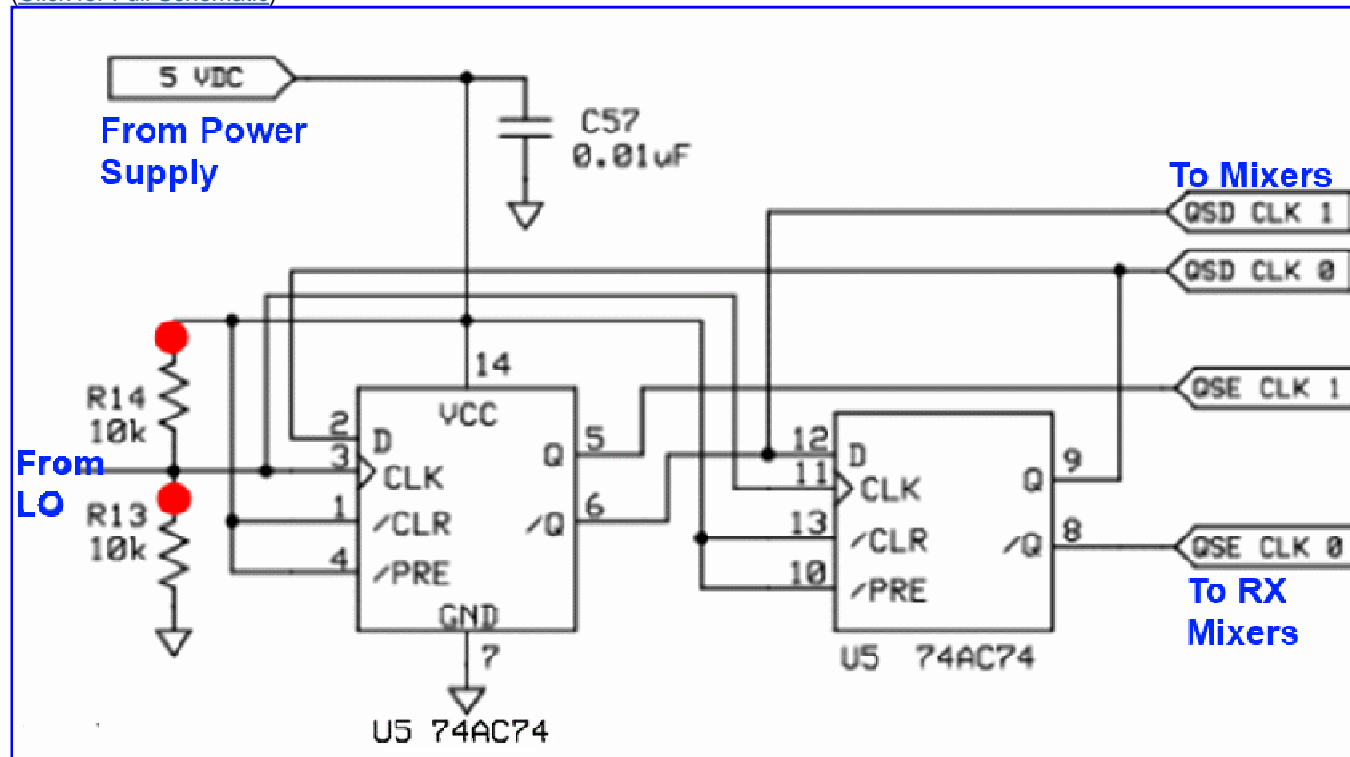
The signals are "in quadrature", that is, they are 90° out of phase with each other. These are provided to the TX and RX mixer stages as clocking signals. They are called out on testpoints marked "QSD Clk (1 or 2)", for the I and Q signals to mix down the incoming "chunk" of RF, and "QSE Clk (1 or 2)", for the I and Q signals which mix up the PC's line out signals.

[\(go directly to build notes\)](#)

Dividers Schematic

(Resistor testpoints (hairpin, top, or left-hand lead), as physically installed on the board, are marked in the schematic with red dots)

(Click for Full Schematic)




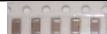
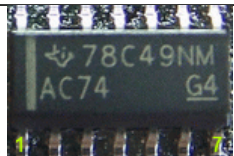
(above schematic has clickable areas that can be used for navigation)

(go directly to build notes)

Dividers Bill of Materials

Stage Bill of Materials

(resistor images and color codes courtesy of [Wilfried, DL5SWB's R-Color Code program](#))

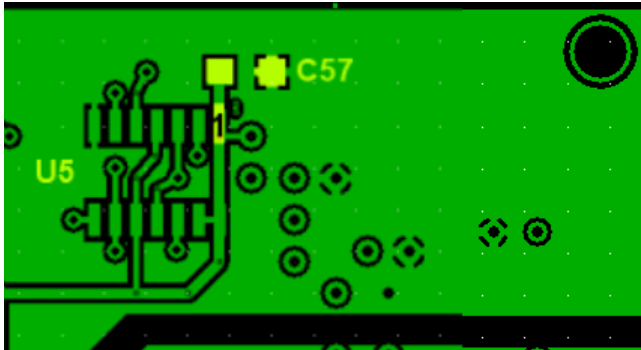
Check	Count	Component	Marking	Category
<input type="checkbox"/>	2	10 k 1/4W 1%	br-blk-blk-r-br 	1/4W
<input type="checkbox"/>	1	0.01 uF	(smt) 	SMT 1206
<input type="checkbox"/>	1	74AC74 Dual D FF	 74AC74	SOIC-14

Dividers Summary Build Notes

- Install SMT Components
- Install Topside Components
- [Test the Stage](#)

Dividers Detailed Build Notes

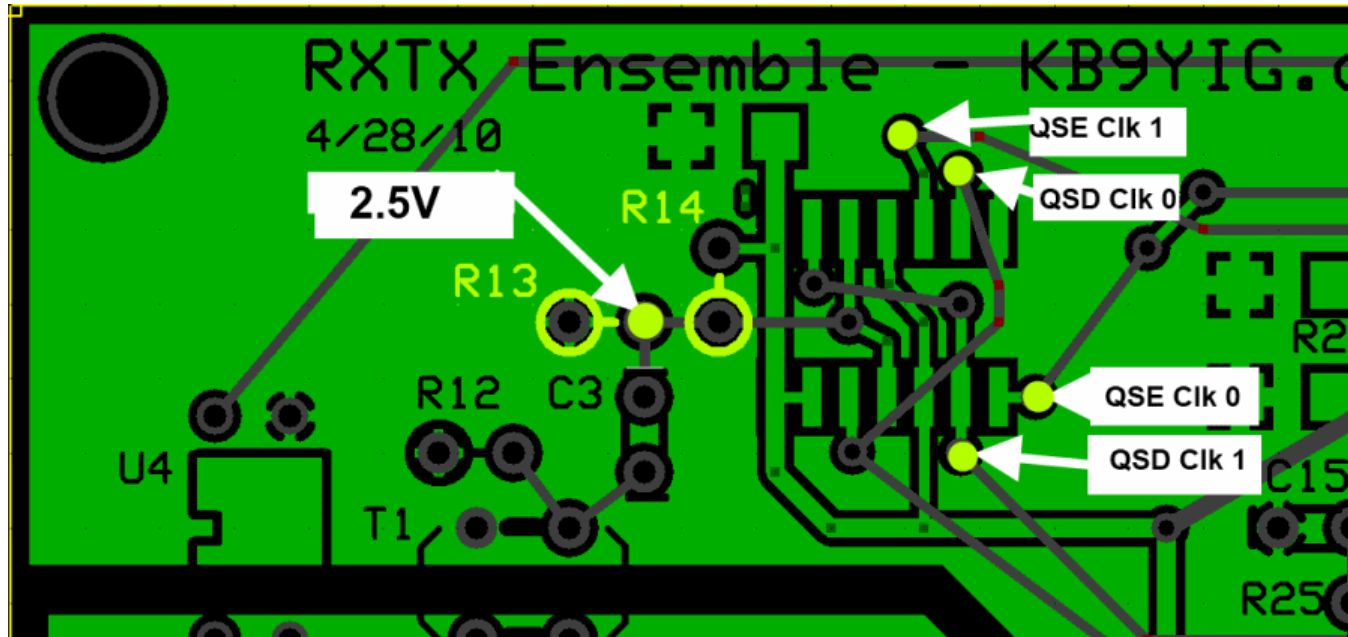
Bottom of the Board



Install SMT Components

Check	Designation	Component	Marking	Category	Orientation	Notes
<input type="checkbox"/>	U05	74AC74 Dual D FF	74AC74 78C49NM AC74 G4	SOIC-14	AC74 78C49NM G4	Take ESD precautions Markings vary - look for "AC74"
<input type="checkbox"/>	C57	0.01 uF	(smt)	SMT 1206		

Top of the Board

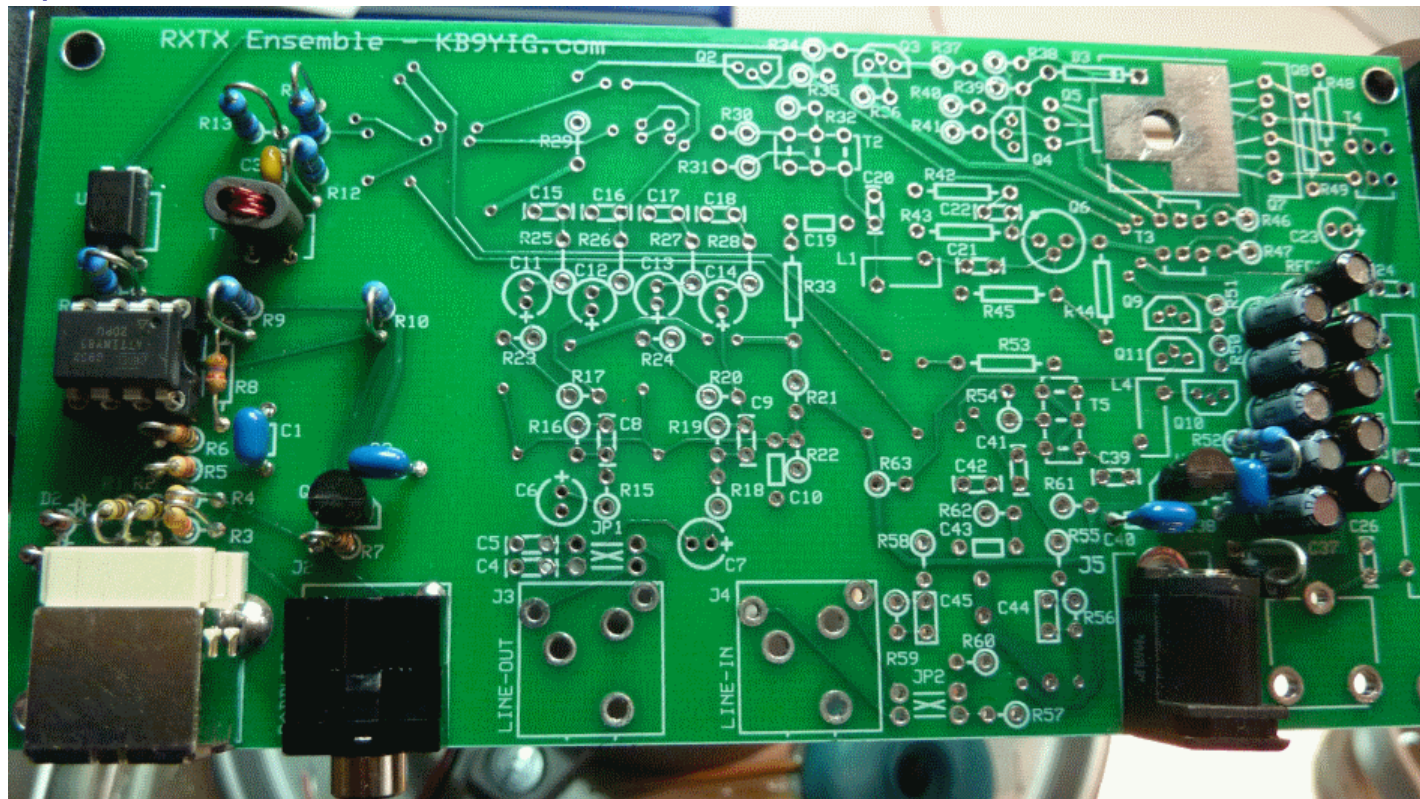


Install Topside Components

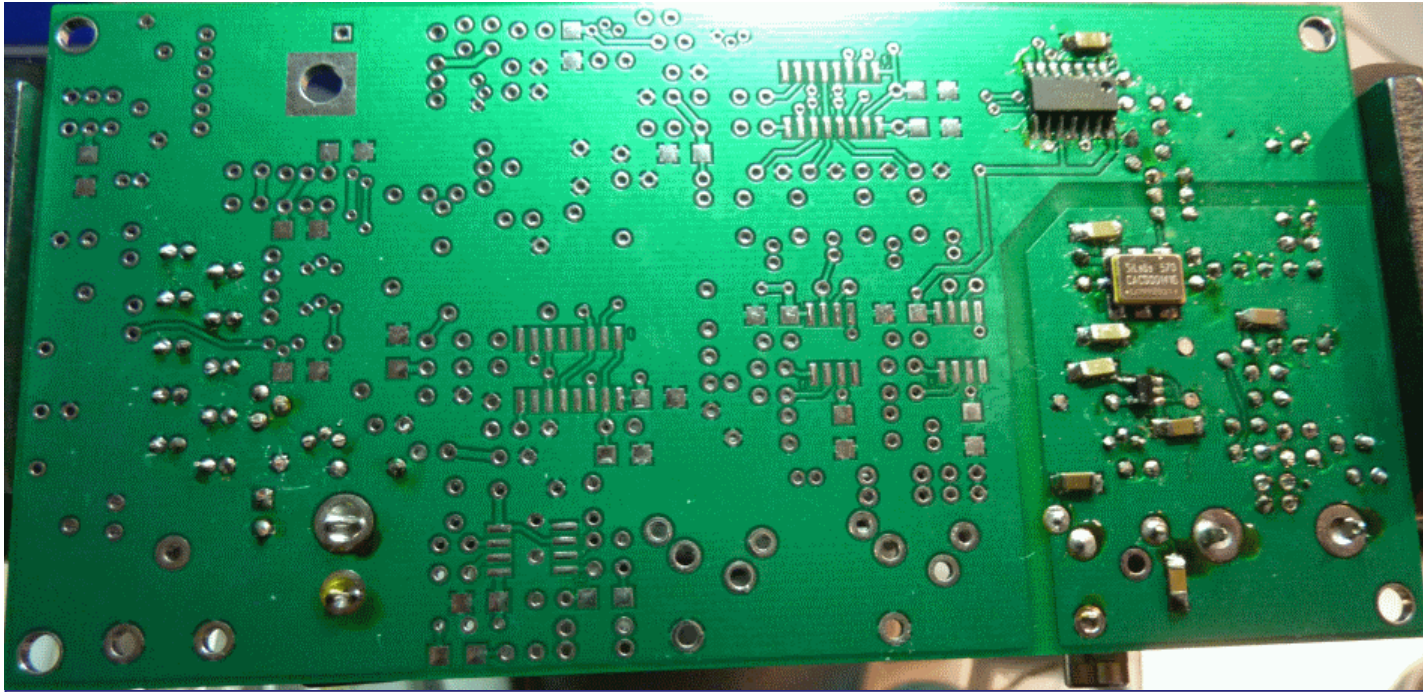
Check	Designation	Component	Marking	Category	Orientation	Notes
<input type="checkbox"/>	R13	10 k 1/4W 1%	br-blk-blk-r-br 	1/4W	W-E	
<input type="checkbox"/>	R14	10 k 1/4W 1%	br-blk-blk-r-br 	1/4W	S-N	

Dividers Completed Stage

Top of the Board



Bottom of the Board



Dividers Testing

Current Draw (13V bus)

Test Setup

Power the board on the 13v power jack and measure the current draw at the power input

Test Measurements

Testpoint	Units	Nominal Value	Author's	Yours
Current draw (13V only)	mA	< 20	13.2	

Voltage Divider Test

Test Setup

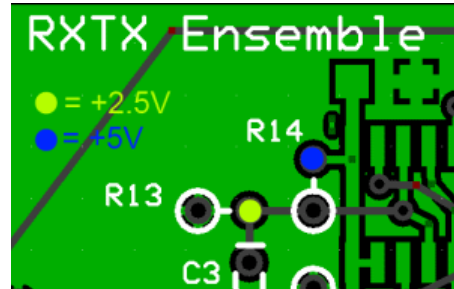
Connect the board to 13V power

Measure following voltages WRT (regular) ground (at R50 hairpin):

- At the hairpin of R13 (the junction of the R13/R14 voltage divider). You should measure approximately one-half the +5V bus value.
- At the hairpin of R14. You should measure the 5V rail voltage

Troubleshooting the Voltage Divider

If you do not get the expected R13 value you expect, the possibilities are most likely that you have a short or you have mounted the wrong resistor value(s). For the latter case, you may want to use the [utility Voltage Divider Calculator](#) to enter your actual R13 value (V_{out}) and see what resistance values might produce that voltage.



Test Measurements

Testpoint	Units	Nominal Value	Author's	Yours
R13 hairpin (wrt regular ground)	Vdc	+2.5	2.47	
R14 hairpin (wrt regular ground)	Vdc	+5	4.94	

Divider Output

Test Setup

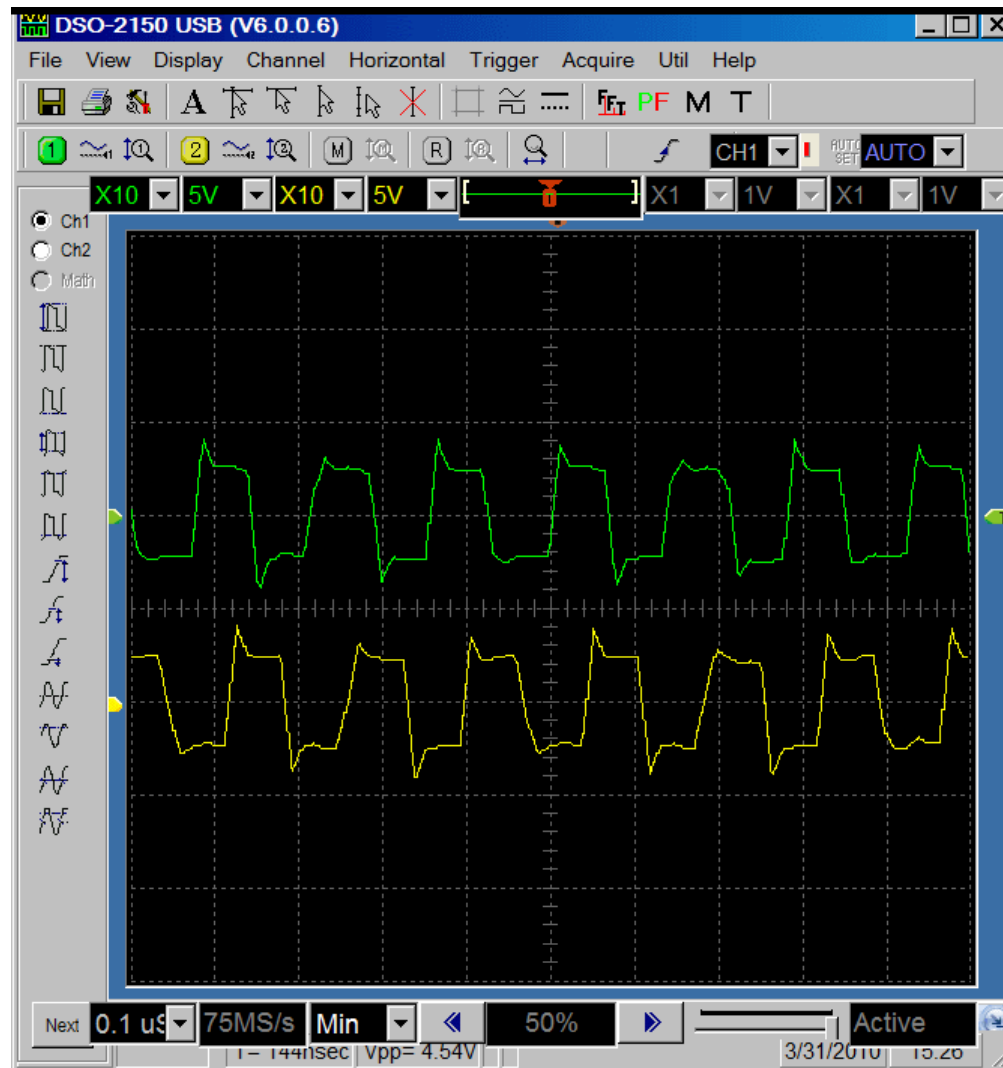
Plug in the USB cable, power up the Ensemble board, start up CFGSR or the SDR Program, and select a center frequency of 7.040 MHz

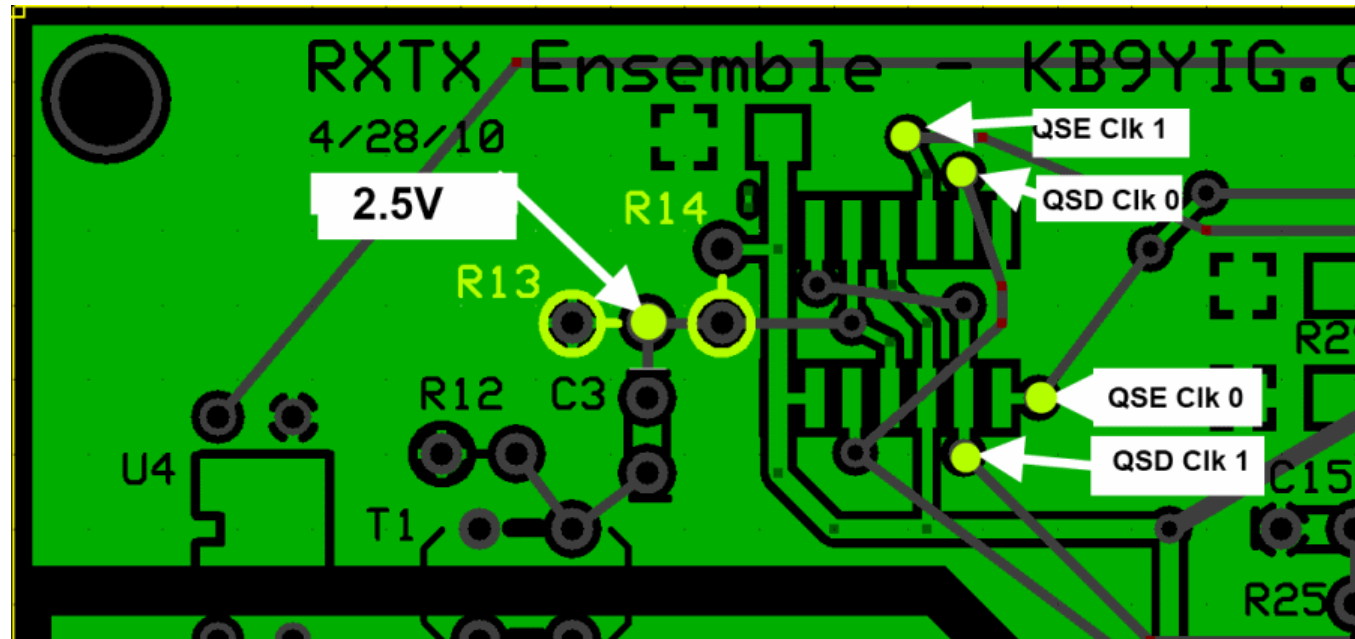
Using a frequency measuring device (e.g., freq counter or HF radio), measure the output of the dividers. The frequency should be one -quarter of the local oscillator frequency and should be the center frequency selected in CFGSR or the SDR program.

For example, if the desired center frequency is 7.040 MHz, the putput at each of the four clock outputs should be 7.040MHz (corresponding to a Local Oscillator output of 28.160 MHz).

If you have a scope, probe one set of clock outputs (QSE or QSD). You should see two identical waveforms, 90 degrees out of phase with one another.

(the image below is from a USB scope, pushed beyond its meager limits to display the two 7.040 MHz square waves in quadrature!)





Test Measurements

Testpoint	Units	Nominal Value	Author's	Yours
QSE Clk 0	MHz	7.040	7.04	
QSE Clk 1	MHz	7.040	7.04	
QSD Clk 0	MHz	7.040	7.04	
QSD Clk 1	MHz	7.040	7.04	

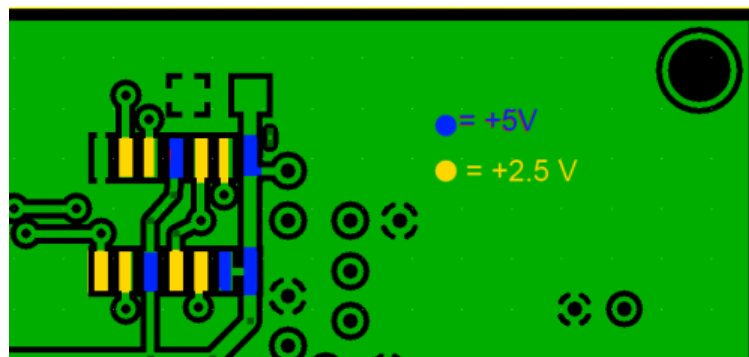
IC Pin Voltage Tests

Test Setup

If you do not get results expected in the preceding tests, connect the USB cable, power up the board and measure the pin voltages on U5, per the graphic showing blue test points for +5 Vdc and yellow test points for 2.5 Vdc. Keep in mind that there will be some variation on the 2.5V pins, for example pins 11 and 13, which will have some AC component to them from the LO.

These voltages are measured WRT regular ground

Note: the Local Oscillator must be running under USB power AND the dividers must be running under 13V power for the measurements below. If the USB is not connected, measurements will be incorrect.



Test Measurements

Testpoint	Units	Nominal Value	Author's	Yours
Pin 1 (blue point)	Vdc	+5	4.94	
Pin 2 (yellow point)	Vdc	+2.5	2.45	
Pin 3 (yellow point)	Vdc	+2.5	2.47	
Pin 4 (blue point)	Vdc	+5	4.94	
Pin 5 (yellow point)	Vdc	+2.5	2.44	
Pin 6 (yellow point)	Vdc	+2.5	2.45	
Pin 7 (regular ground)	Vdc	0	0	
Pin 8 (yellow point)	Vdc	+2.5	2.44	
Pin9 (yellow point)	Vdc	+2.5	2.44	
Pin 10 (blue point)	Vdc	+5	4.94	
Pin 11 (yellow point)	Vdc	+2.5	2.47	
Pin 12 (yellow point)	Vdc	+2.5	2.44	
Pin 11 (blue point)	Vdc	+5	4.94	
Pin 14 (blue point)	Vdc	+5	4.94	

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